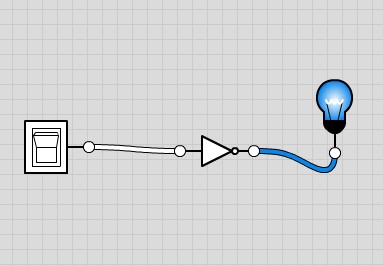
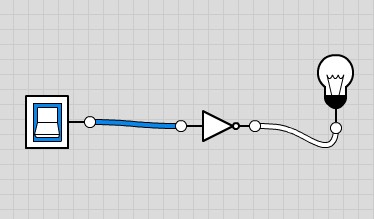
# Name : ABDUL GHANI KHAN

**Section: BCS-2A2**

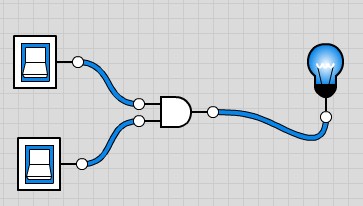
**Roll-No: 22P-9037**

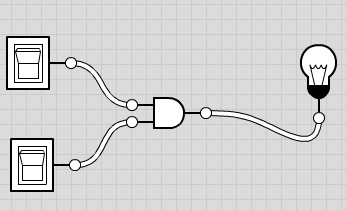
# Logic NOT Gate:



|  |  |
| --- | --- |
| **Input** | **output** |
| 0 | 1 |
| 1 | 0 |

# Logic AND Gate:

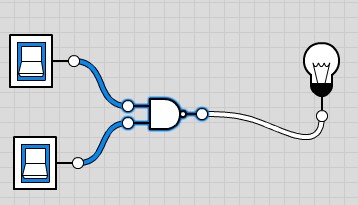


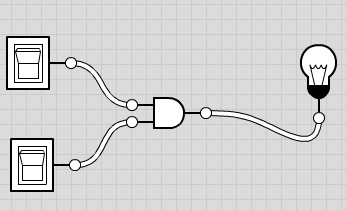
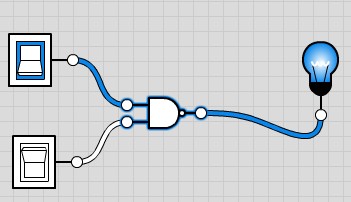


|  |  |  |
| --- | --- | --- |
| **input(A)** | **input(B)** | **output(X)** |
| 0 | 1 | 0 |
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

|  |  |  |
| --- | --- | --- |
| **Input(A)** | **input(B)** | **output(X)** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

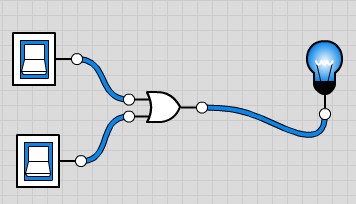
# Logic NAND Gate:

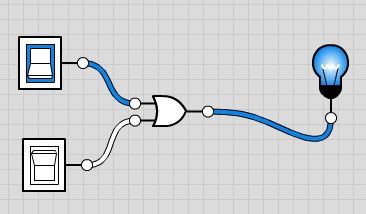
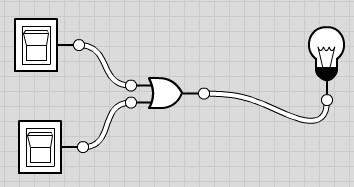




# Logic OR Gate:

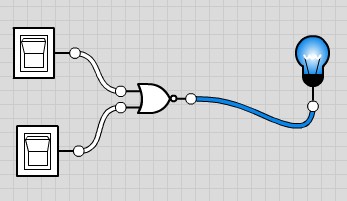
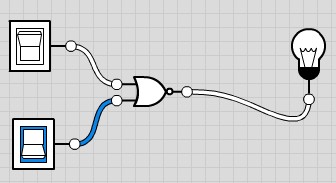
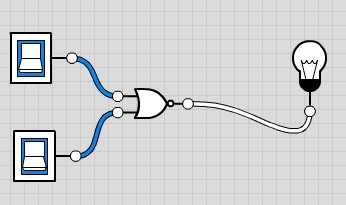
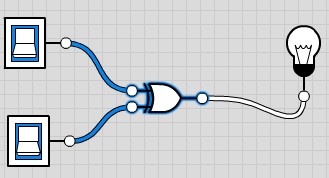
|  |  |  |
| --- | --- | --- |
| **Input(A)** | **Input(B)** | **Output** |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |
| 0 | 0 | 0 |





# Logic NOR Gate:

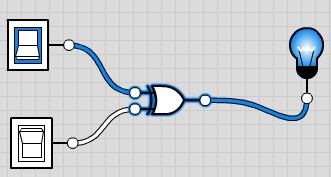
The Logic NOR Gate is a combination of the digital logic OR gate and an inverter or NOT gate connected together.



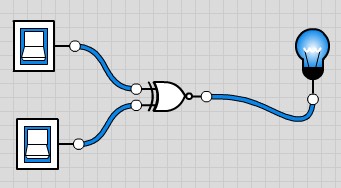
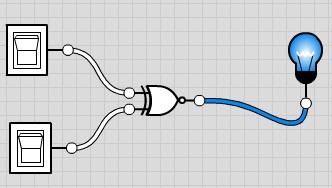
|  |  |  |
| --- | --- | --- |
| **Input(A)** | **Input(B)** | **Output** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

# Exclusive-OR Gate:

|  |  |  |
| --- | --- | --- |
| **Input(A)** | **Input(B)** | **Output** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



# Exclusive-NOR Gate:



|  |  |  |
| --- | --- | --- |
| **Input(A)** | **Input(B)** | **Output** |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

